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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,386	02/18/2004	Michael Peters	022193-042810US	4341

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/782,386	PETERS, MICHAEL	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Status of the parent application in the cross reference section of the specification should be updated.

Claim Objections

2. Claims 1 and 11 are objected to because of the following informalities:

Claim 1 recites the limitations "the memory" and "said memory". Claim 11 recites the limitation "said memory". While it can be understood that the antecedent basis for the limitations is "a synchronous memory" recited in the preamble, as that is the only memory recited prior to the limitations, the limitations in the body of the claim should be changed to include "synchronous". Applicant should also adopt either "the" or "said" to refer to the same synchronous memory for consistency. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "said memory operation". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dosaka et al. (US Patent No. 5,680,363, hereinafter "Dosaka") in view of Kundu (US Patent No. 5,692,148).

7. The amended limitation "a single row cache" can be interpreted in a variety of ways. One such interpretation is a cache having at least a one row, especially when combined with an open ended language "comprising". Another interpretation is a cache that caches data for at least an entire row of data cells in the synchronous memory. Yet another interpretation is a cache that can only hold data for one row of the data cells in the synchronous memory.

8. With respect to claims 1, 11, 12, 22, 23, Dosaka discloses a method for reading data from a memory (figure 22) of the type having data cells arranged in rows and columns and having a single row cache (SMA 1 – 4), comprising:

arranging the memory in a symmetrical layout to include a left plurality of N memory portions (LMB) including a left memory block, a central sense amplifier block (dark region between LMB and UMB, see also figure 28, 504 and col. 6, lines 11 – 13), and a right memory

block (UMB); a centrally located single row cache (SMA 1 – 4, SRAMs comprise at least one row or register, an SRAM cache register also holds data from one row of DRAM, col. 5, lines 11 – 13); and a

right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two (figure 22);

receiving an initial command and row address data for reading contents of a row of said memory selected by said row address data (col. 13, lines 28 – 30);

moving said contents of said row into said single row cache (col. 5, lines 11 – 13);

after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and

in response to said "read" command, reading data from said single row cache at a column address specified by said column address data for output by said memory (col. 5, lines 20 – 23).

Dosaka disclose all of the limitations discussed above. However, Dosaka does not specifically disclose that the memory is of synchronous DRAM type. On the other hand, Kundu specifically discloses that synchronous DRAMs (SDRAMs) are faster than DRAMs (Kundu, col. 1, lines 36 – 39).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kundu and Dosaka before him at the time the invention was made, to use the faster SDRAM teachings of Kundu in the memory system of Dosaka, in order to reduce memory access cycle by almost 50% (Kundu, col. 1, lines 39 – 42).

9. Even under narrower interpretation of "a single memory", wherein the cache can only hold data for one row of the data cells in the synchronous memory, it would have been obvious over Dosaka and Kundu. Removing excess components (i.e. extra cache registers) that are not needed is obvious. One skilled in the art would be motivated to remove excess capacity to reduce required real estate as well as to reduce cost.

10. With respect to claims 2 – 4, 7 – 10, 13 – 17, 20 – 21, 24 – 27, the limitations recited in these dependent claims relate to operations of conventional DRAMs that are not novel features of the claimed invention. For example, substantial concurrency between a command and data addresses is a general feature of a conventional DRAM as is the latency of memory outputs. Bank activation and precharging are also present in conventional DRAMs.

11. With respect to claims 5 – 6 and 18 – 19, outputting data from memory after two clock cycles is specifically shown in figure 4a of Kundu. In addition, a person having ordinary skill in the art would have found it obvious to output data from memory after a specific number of clock cycles in accordance with the characteristics desired.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
December 22, 2004

MATTHEW KIM
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